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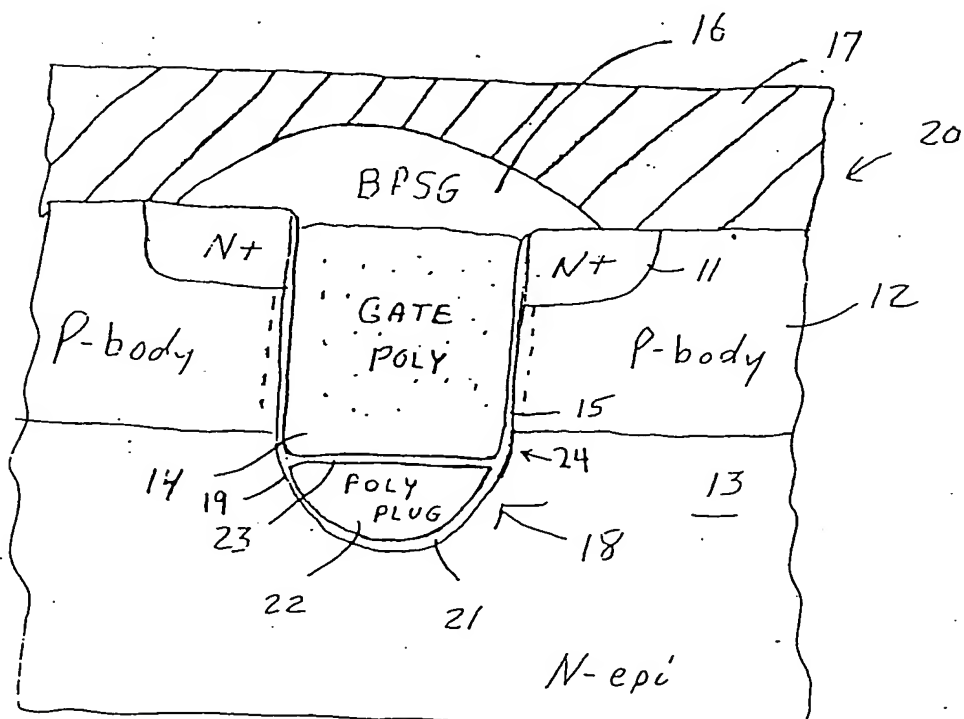
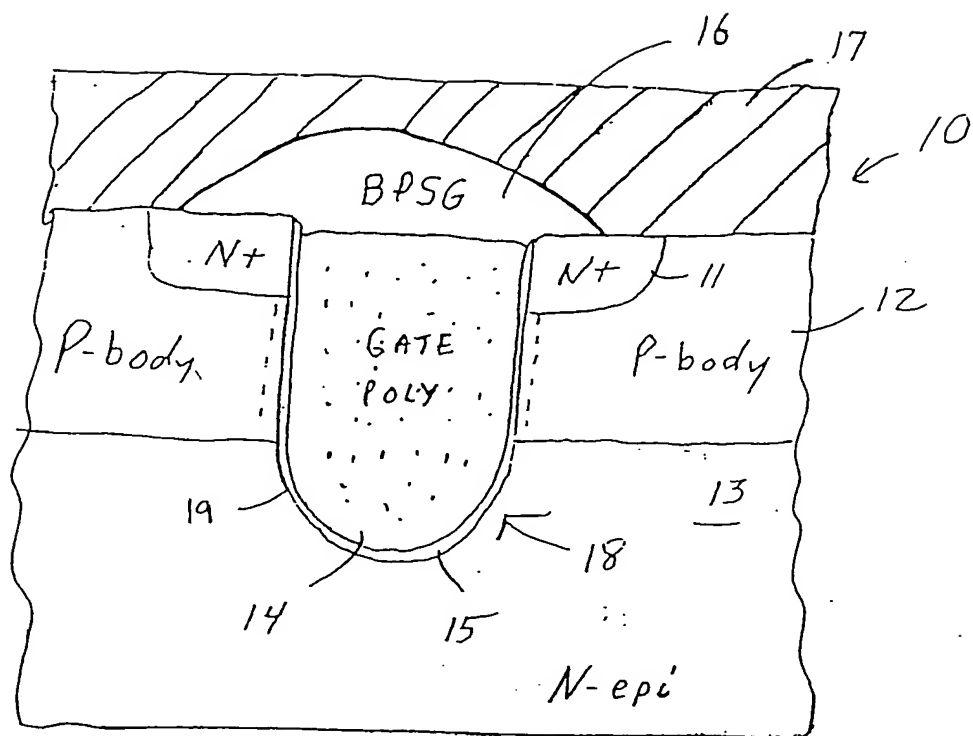
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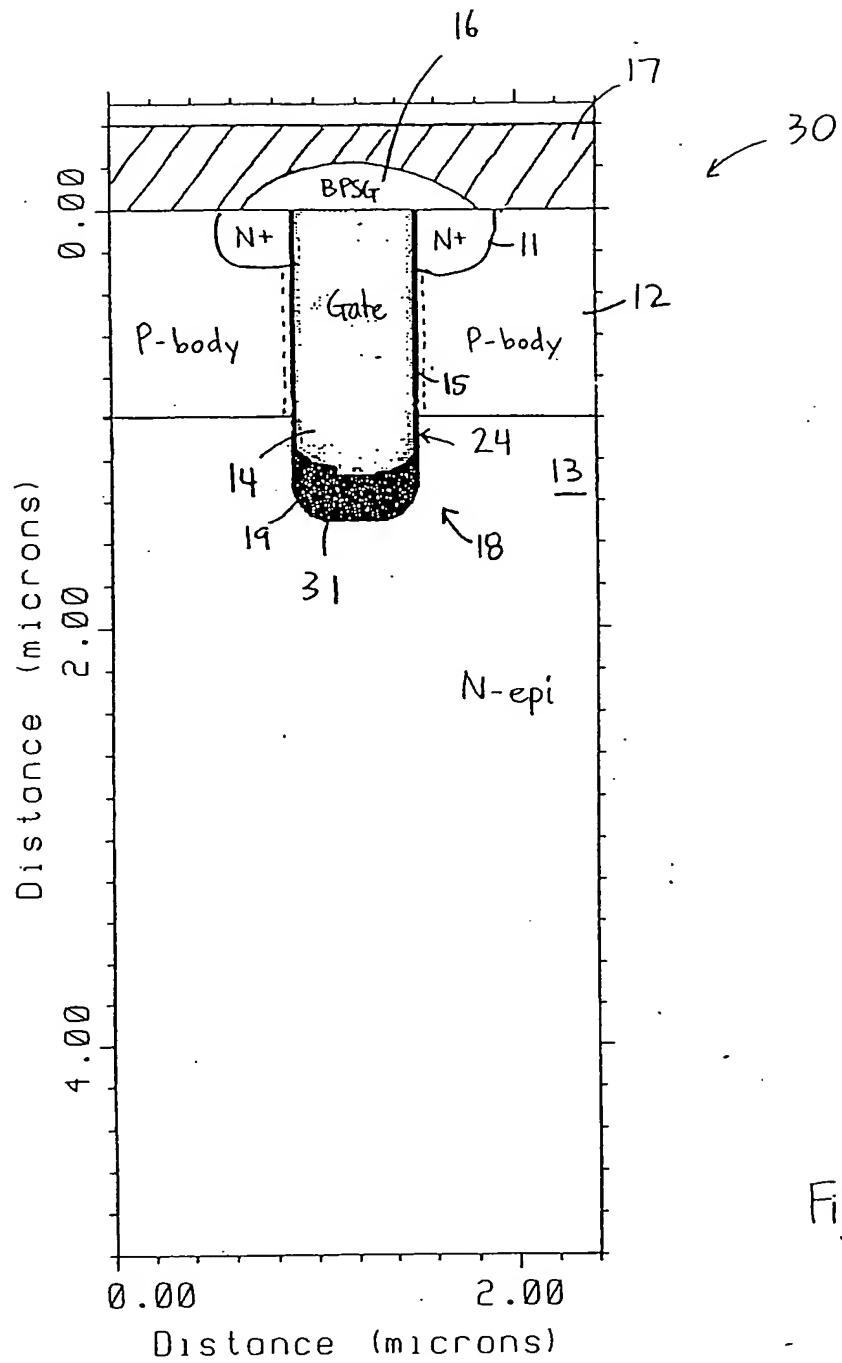


Fig. 3

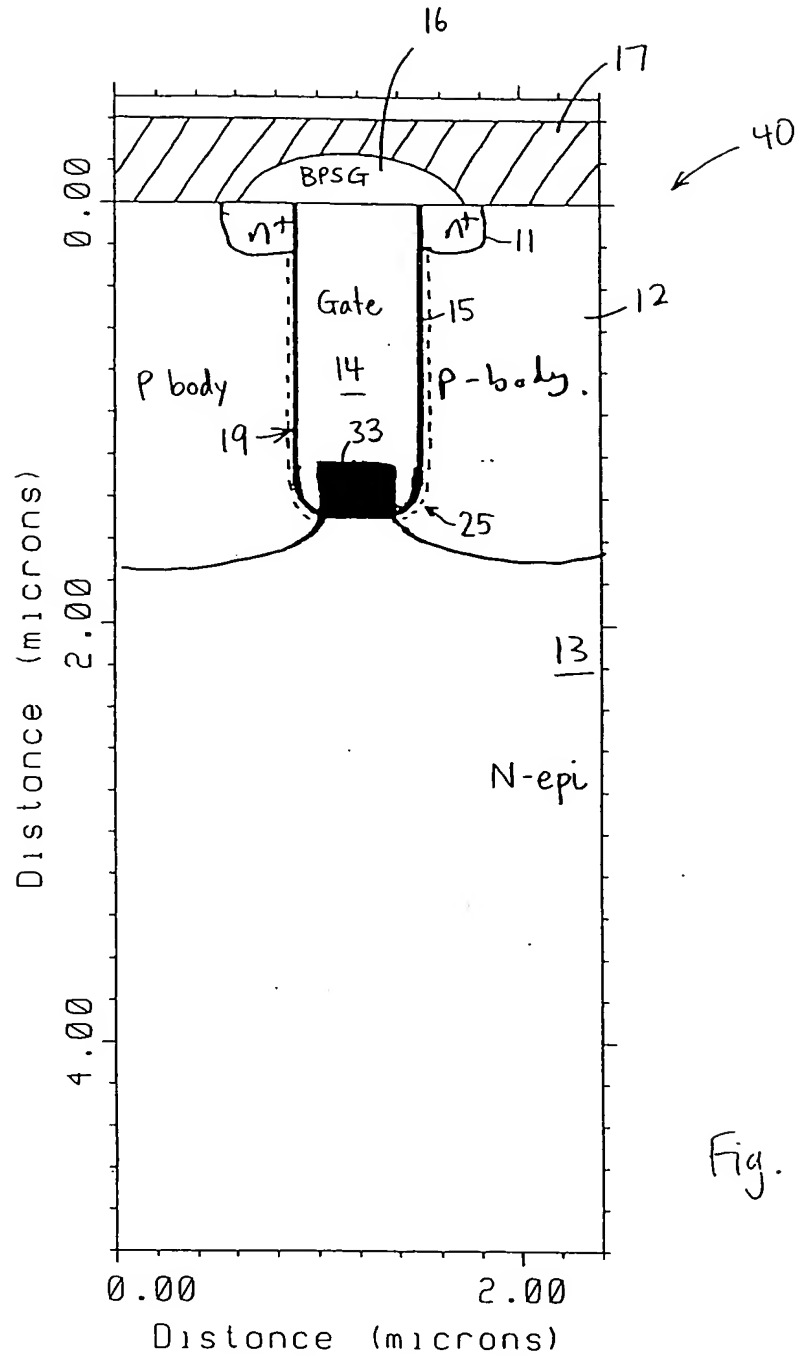


Fig. 4

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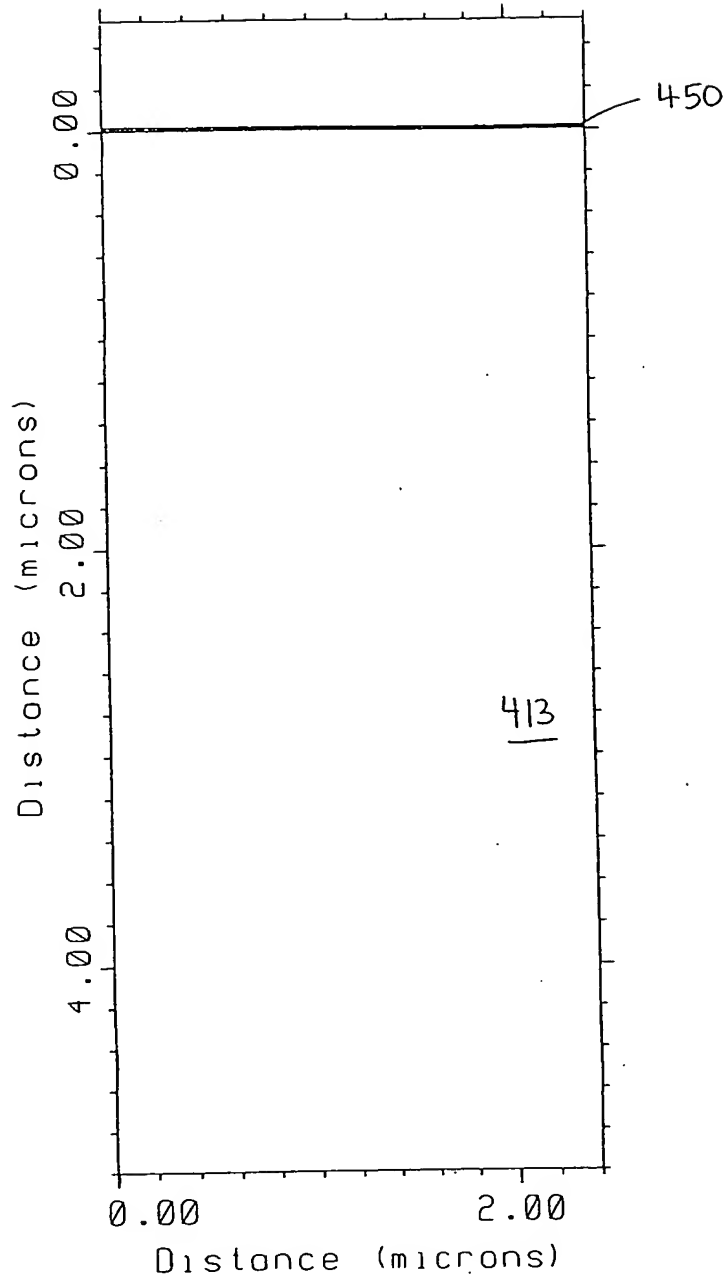


Fig. 5A

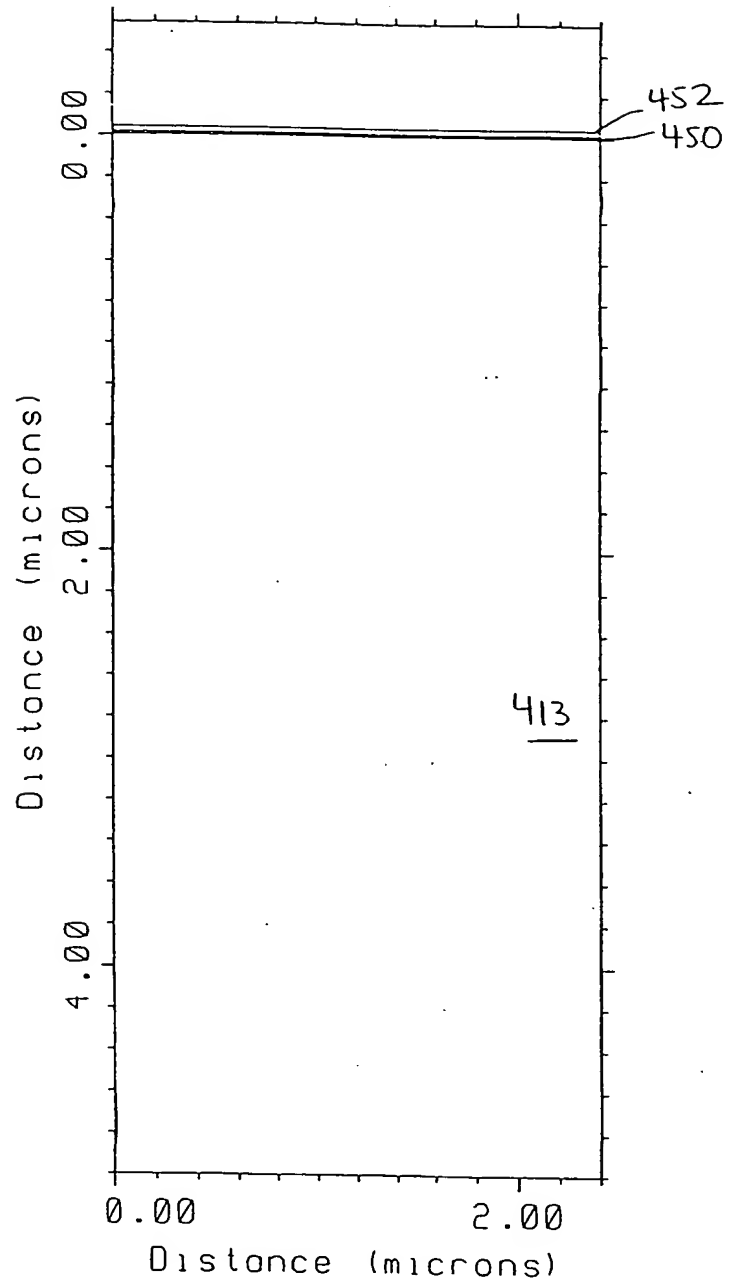


Fig. 5 B.

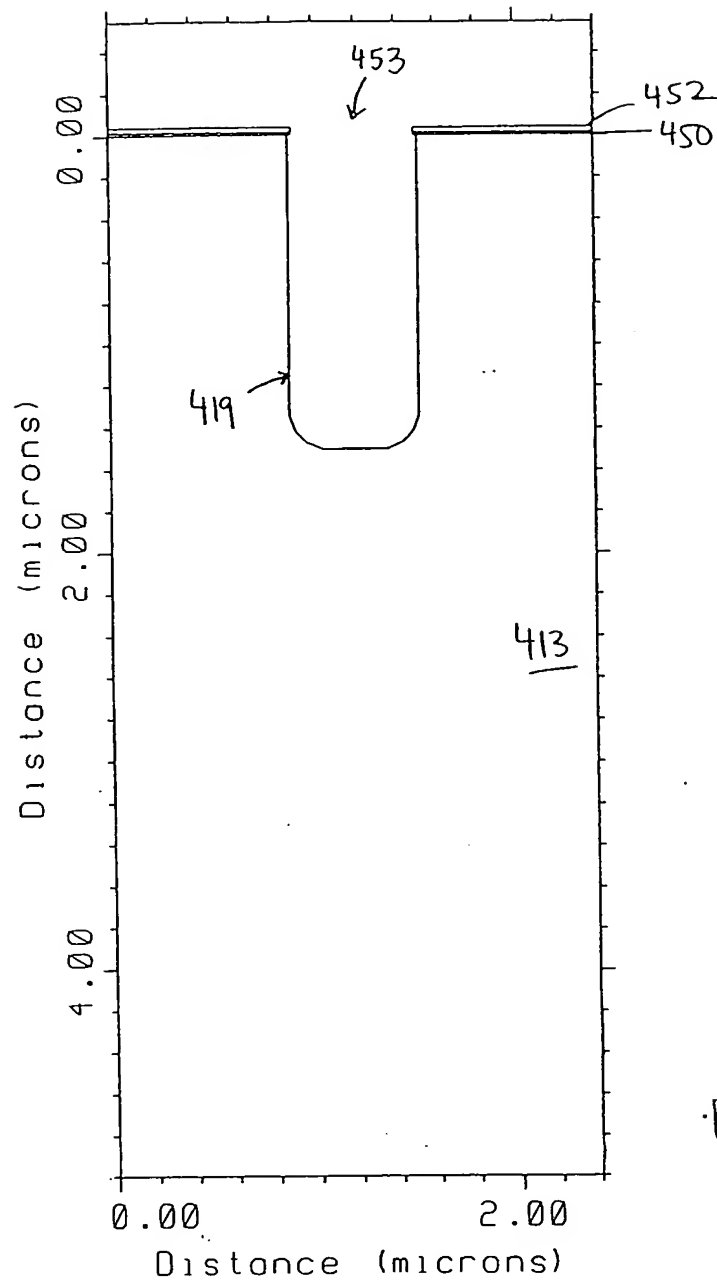


Fig. 5C

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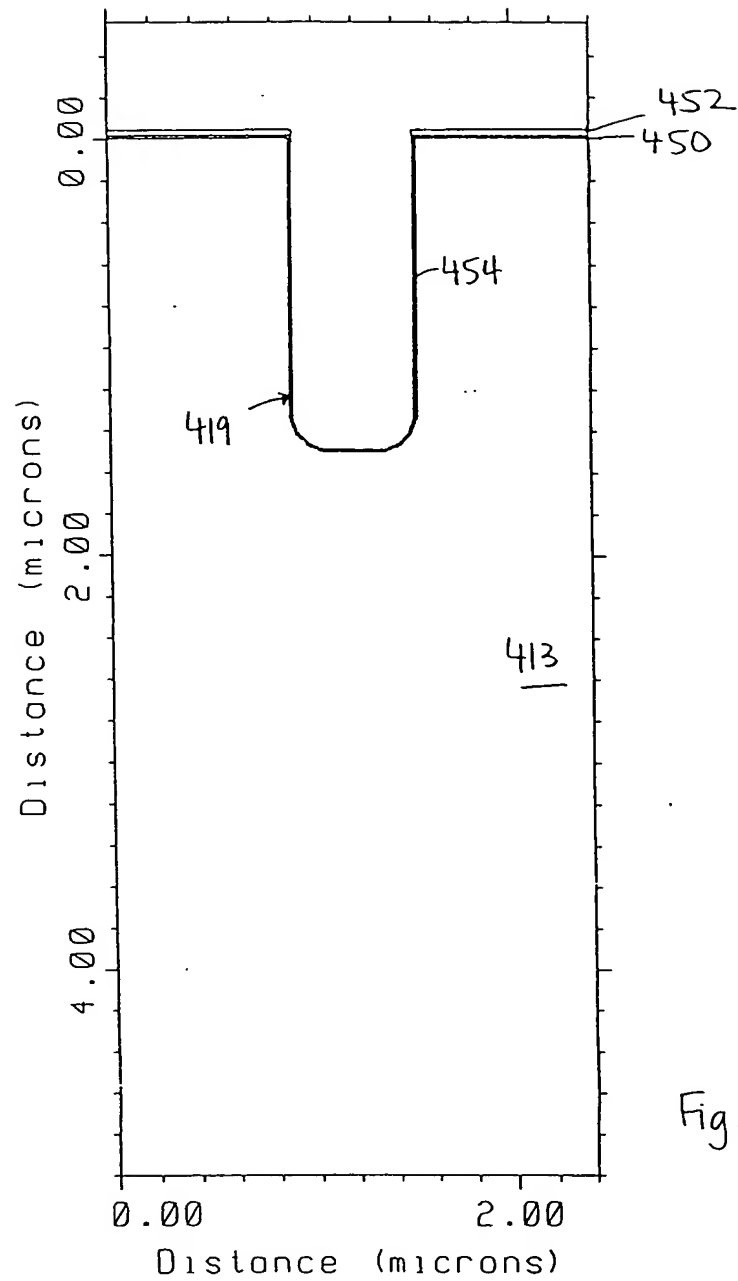


Fig. 5D

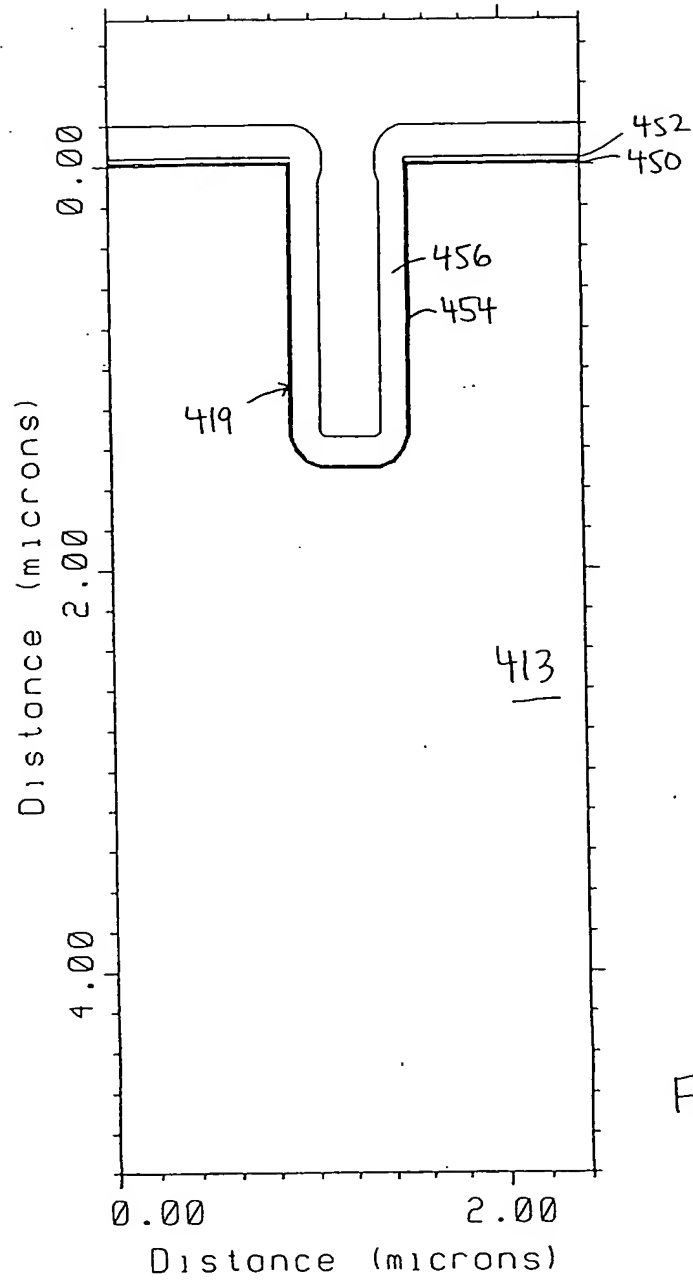


Fig. 5 E

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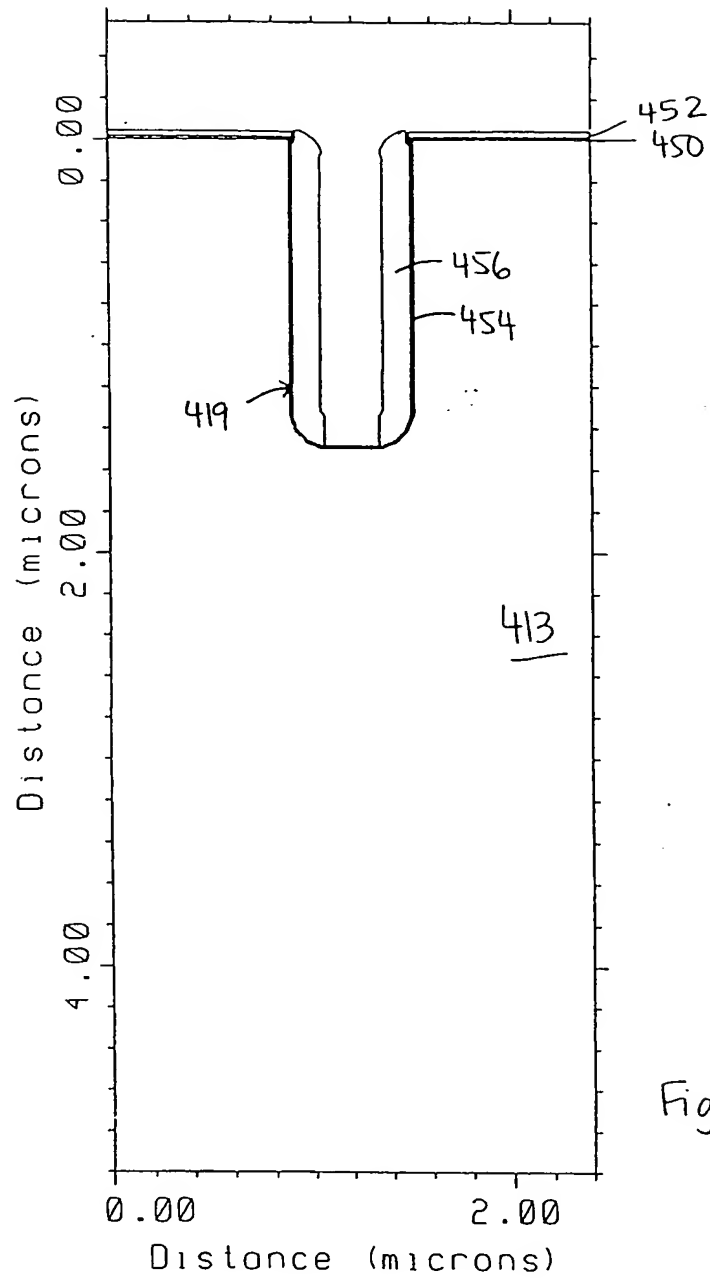


Fig. 5 F

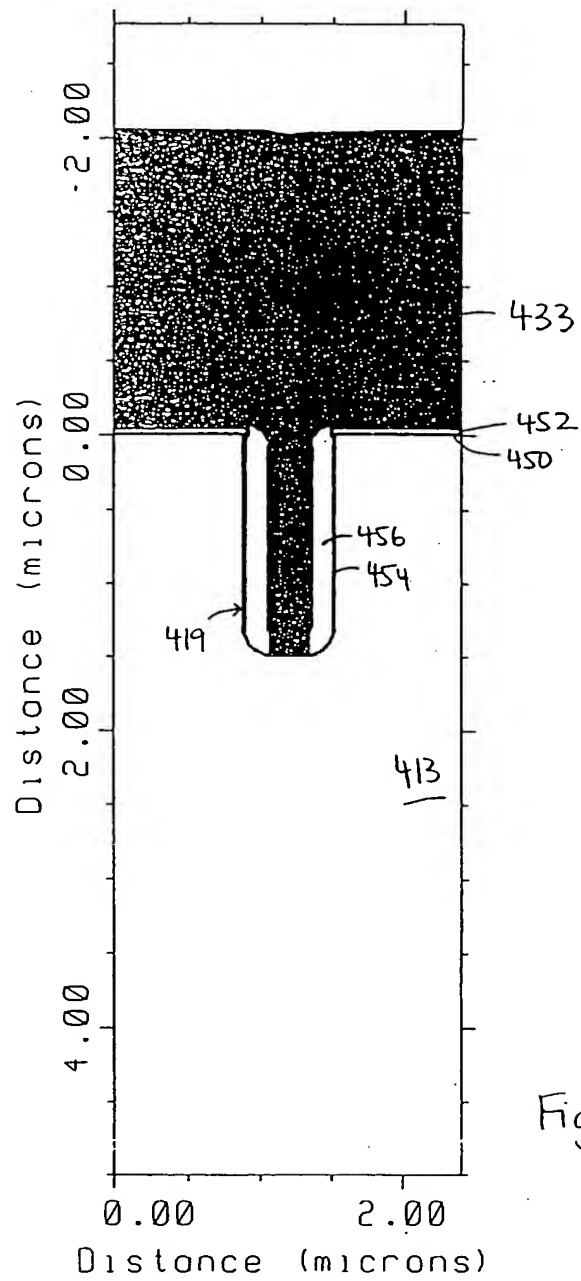


Fig. 5G

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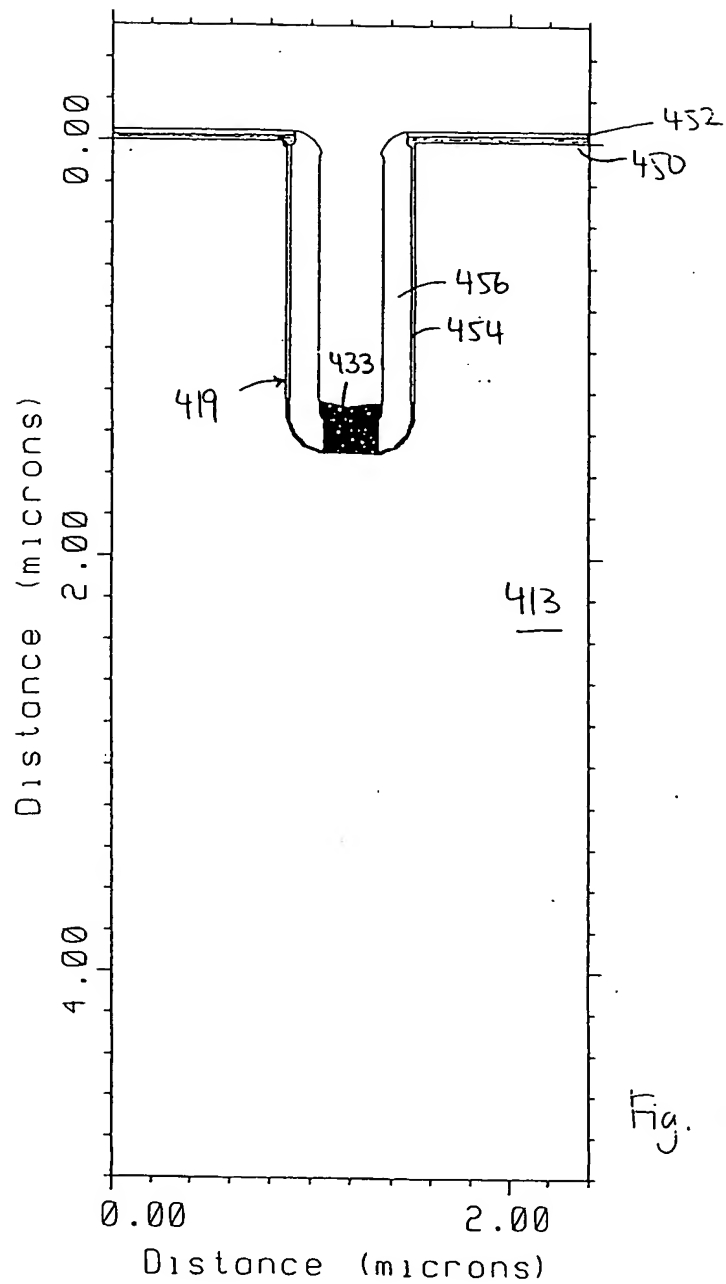


Fig. 5H

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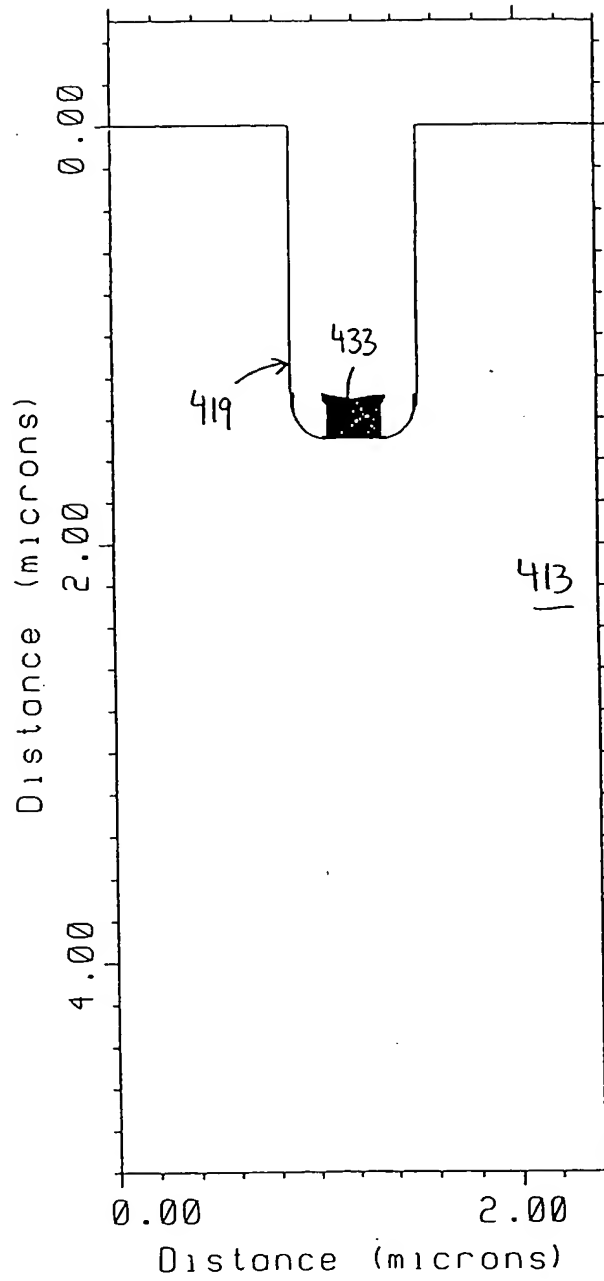


Fig. 5I

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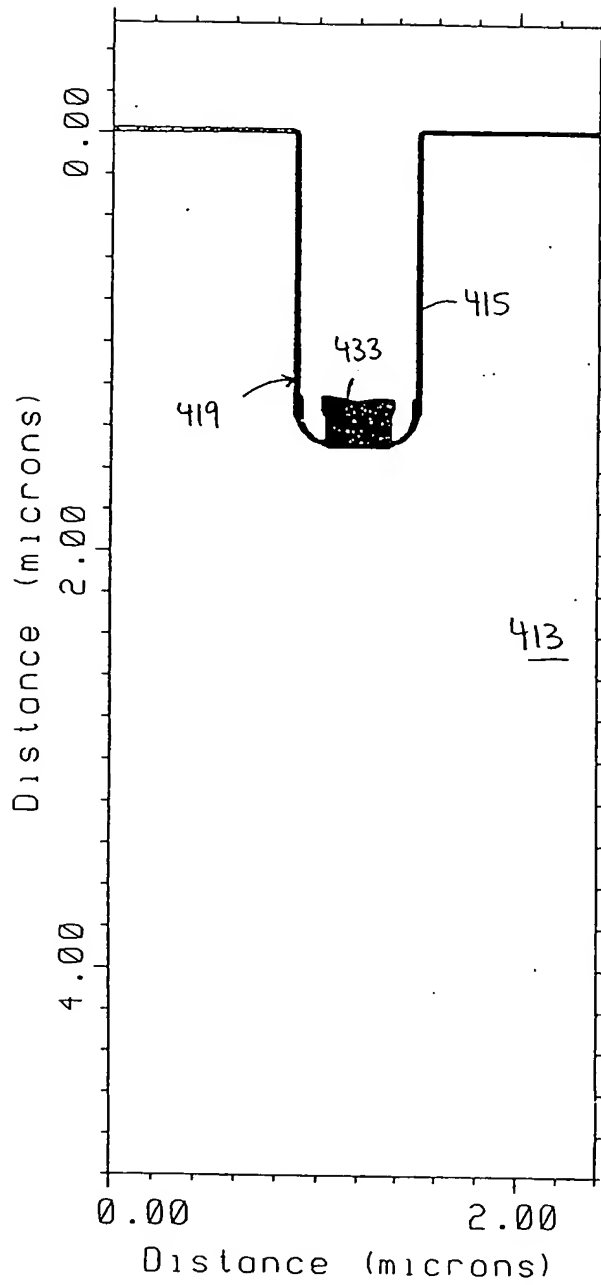


Fig. 5 J

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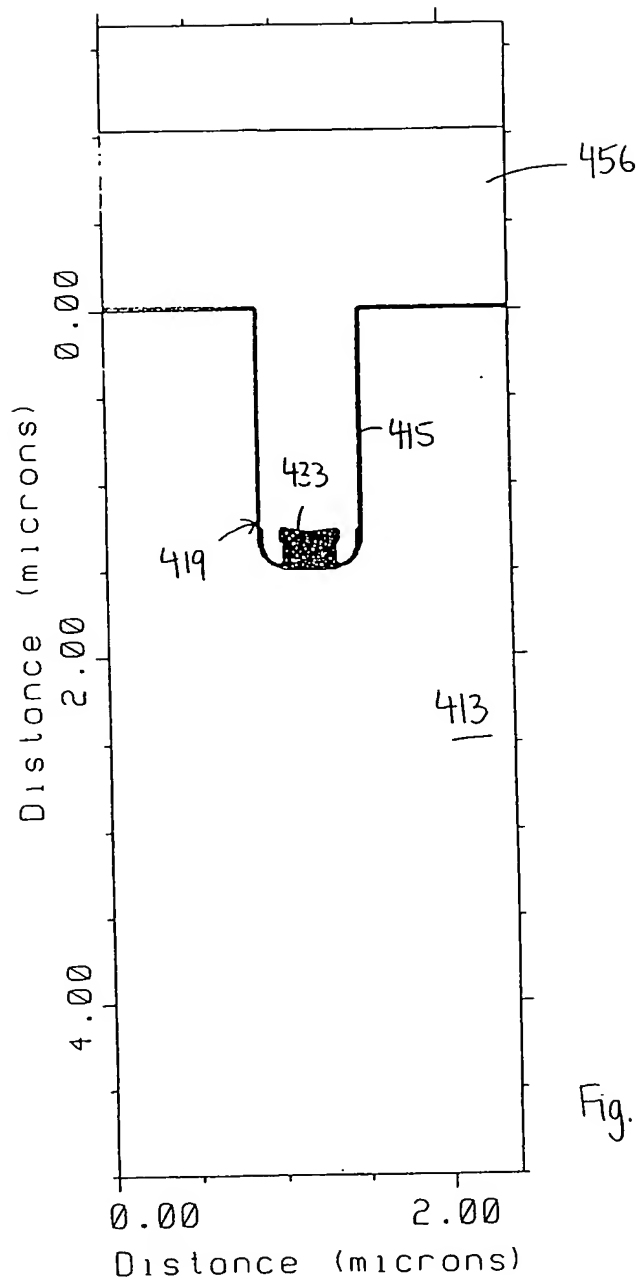


Fig. 5 K

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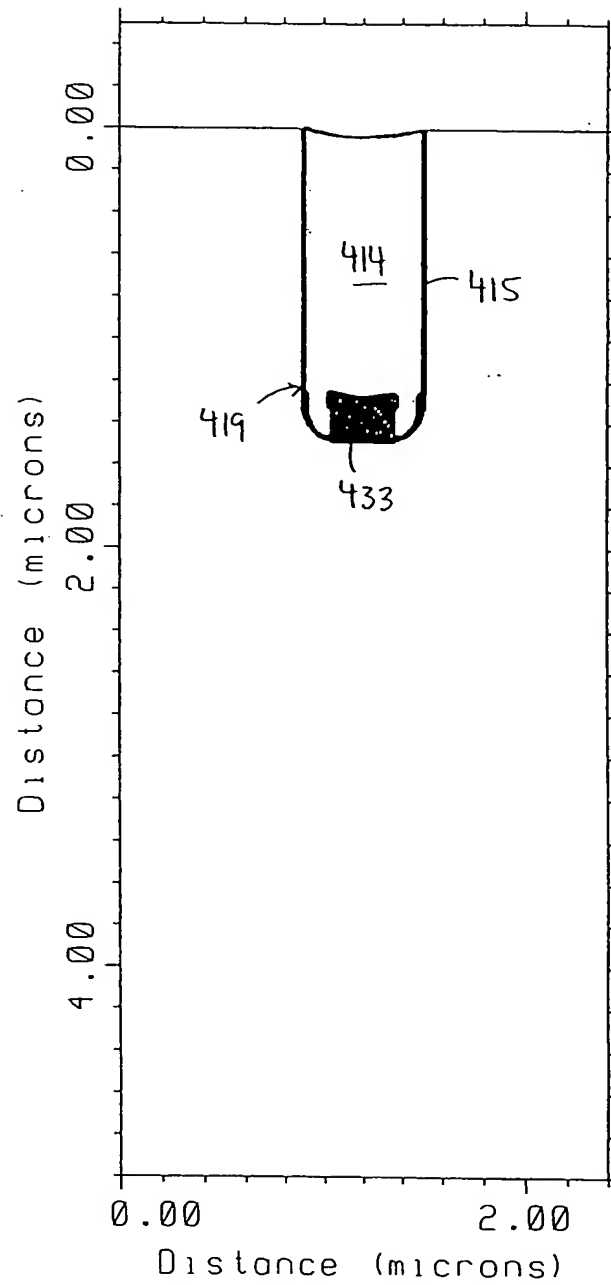


Fig. 5 L

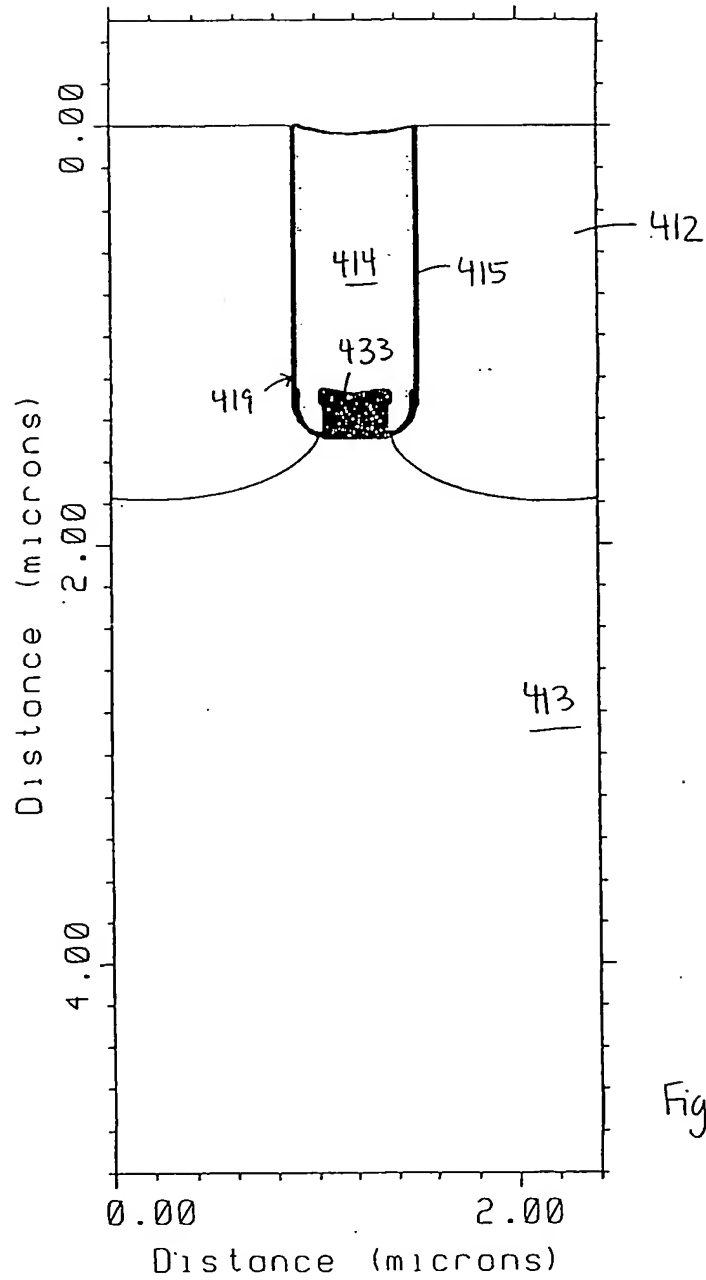


Fig. 5M

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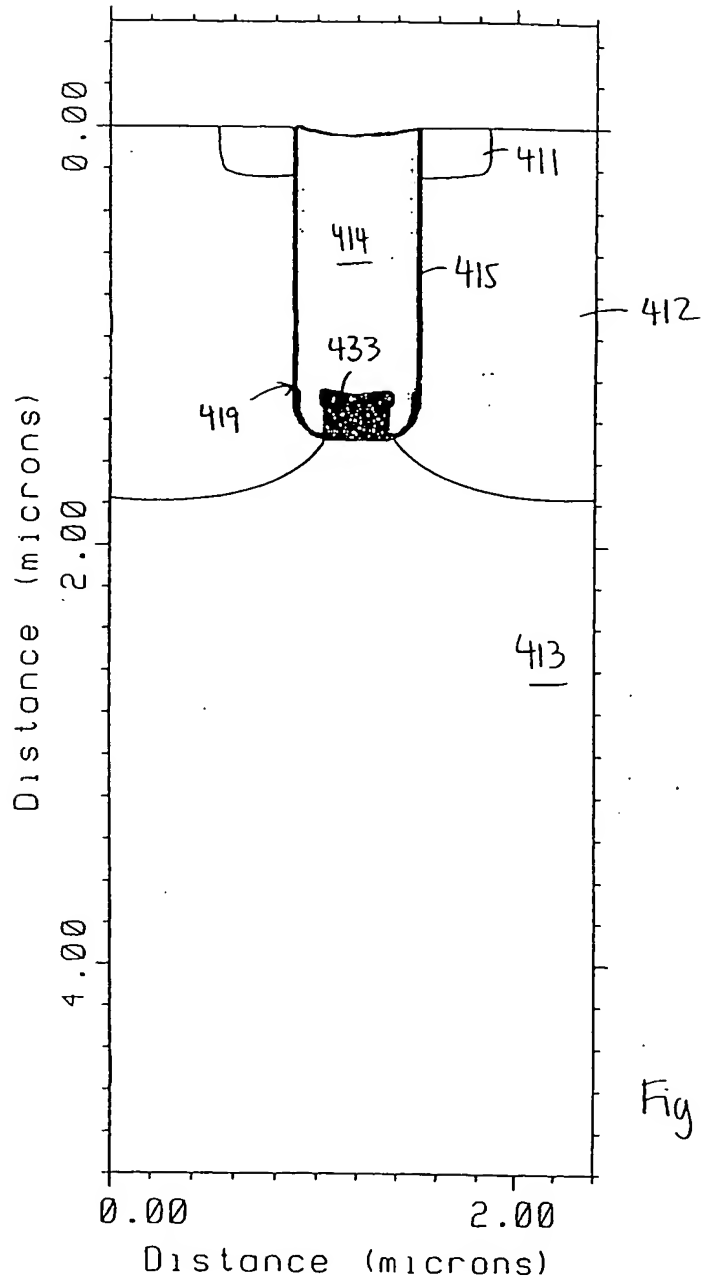


Fig. 5N

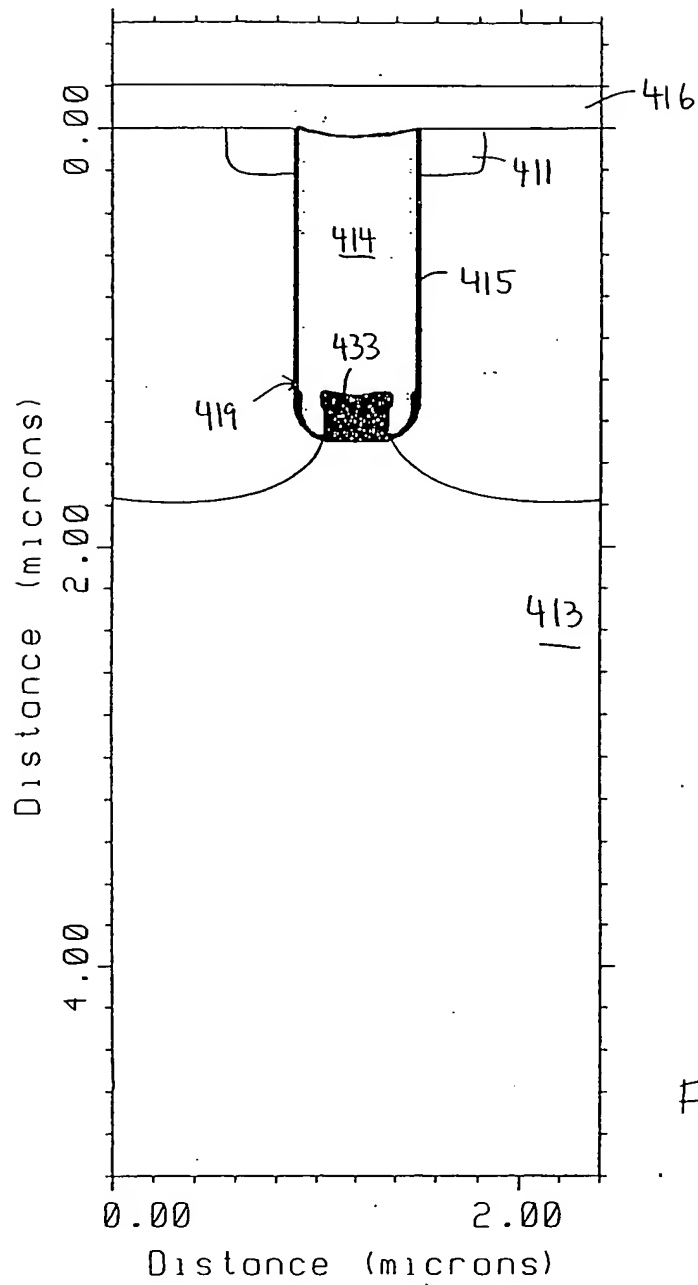


Fig. 50

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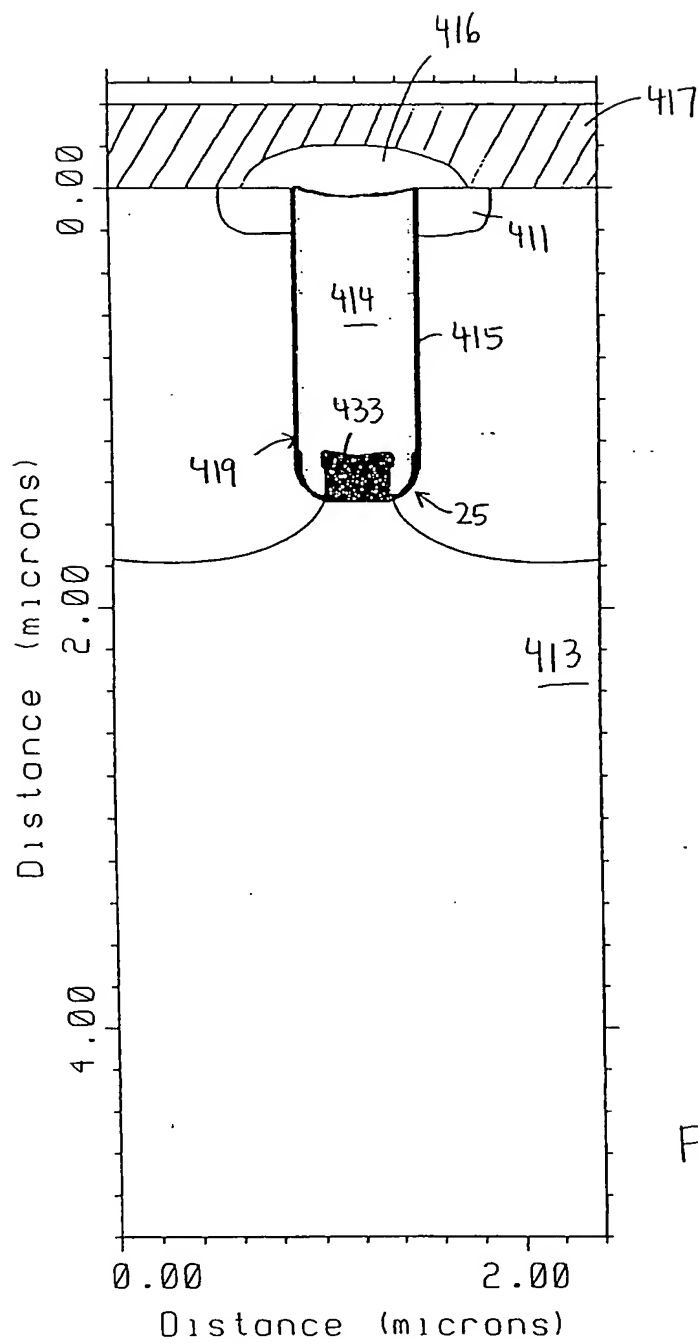
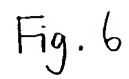


Fig. 5 P



A cross-sectional diagram of a semiconductor device structure. The vertical axis is labeled "Distance (microns)" with values 0.00, 2.00, and 4.00. The horizontal axis is labeled "Distance (microns)" with values 0.00 and 2.00. The structure consists of several layers: a top layer (16) labeled "BPSG", a layer (17) below it, a central "Gate" (14) region, and a "P body" region (19) on the left and "p-body" region on the right. A dashed line (11) indicates the boundary of the p-body. A dashed line (15) indicates the boundary of the gate. A dashed line (13) indicates the boundary of the "N-epi" layer. A dashed line (25) indicates the boundary of the "N" region. A dashed line (73) indicates the boundary of the "N" region. A dashed line (70) indicates the boundary of the "N" region. A dashed line (73) indicates the boundary of the "N" region.

Fig. 7

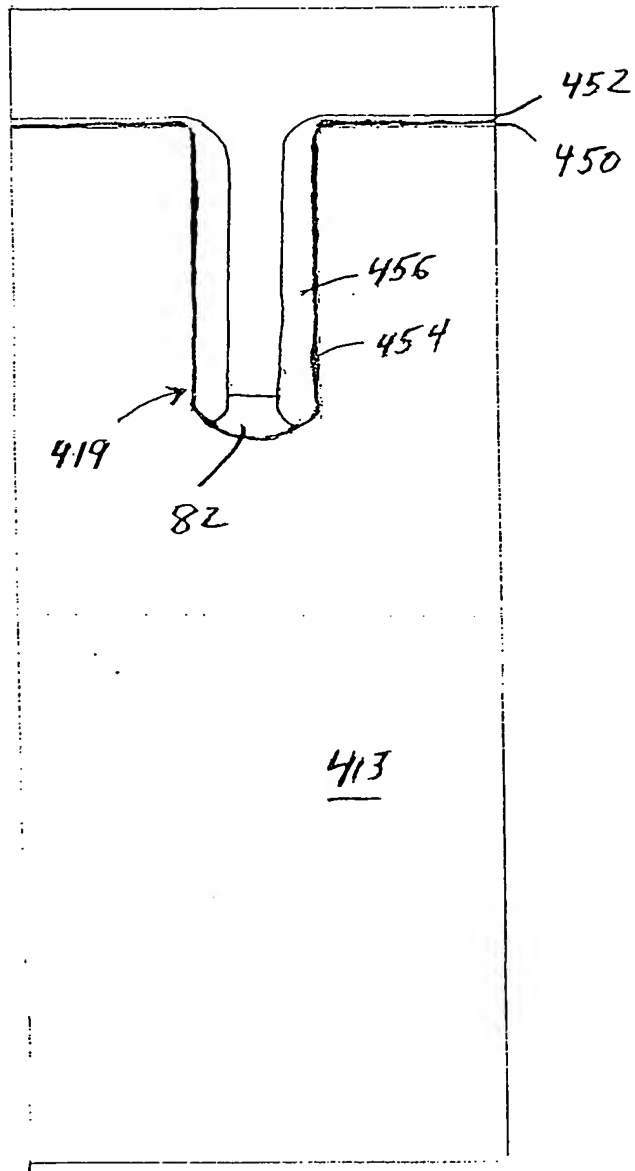
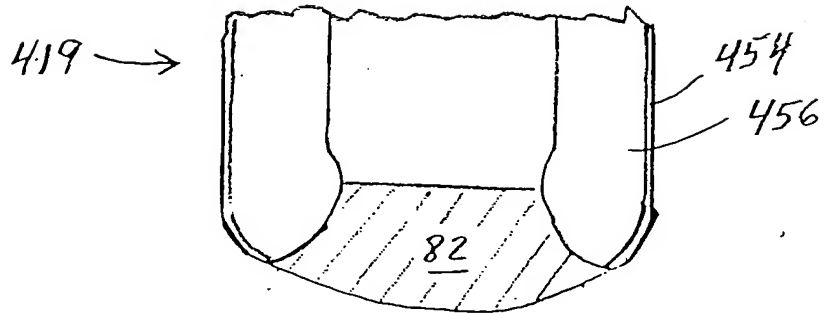
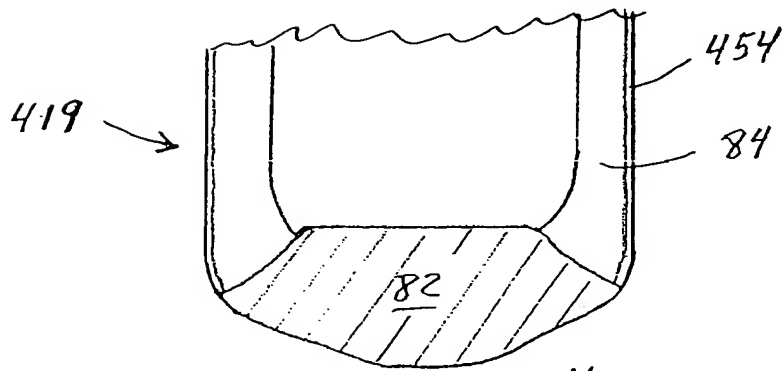


Fig 8



N- Fig. 9A N-



N- Fig. 9B N-

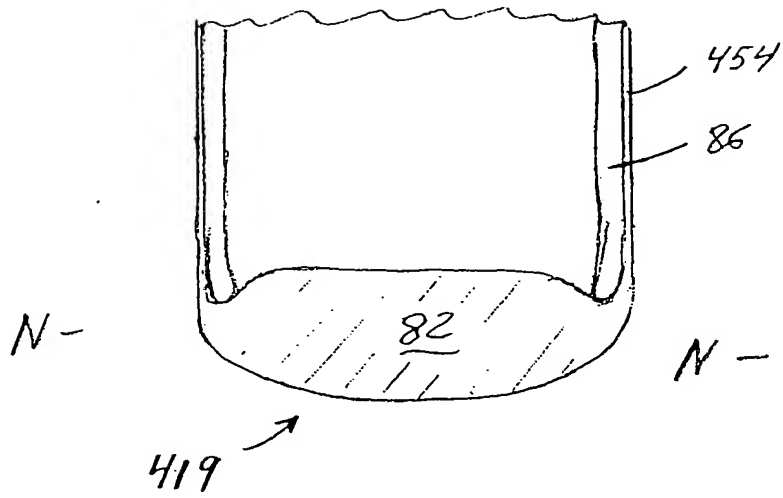


Fig. 9C

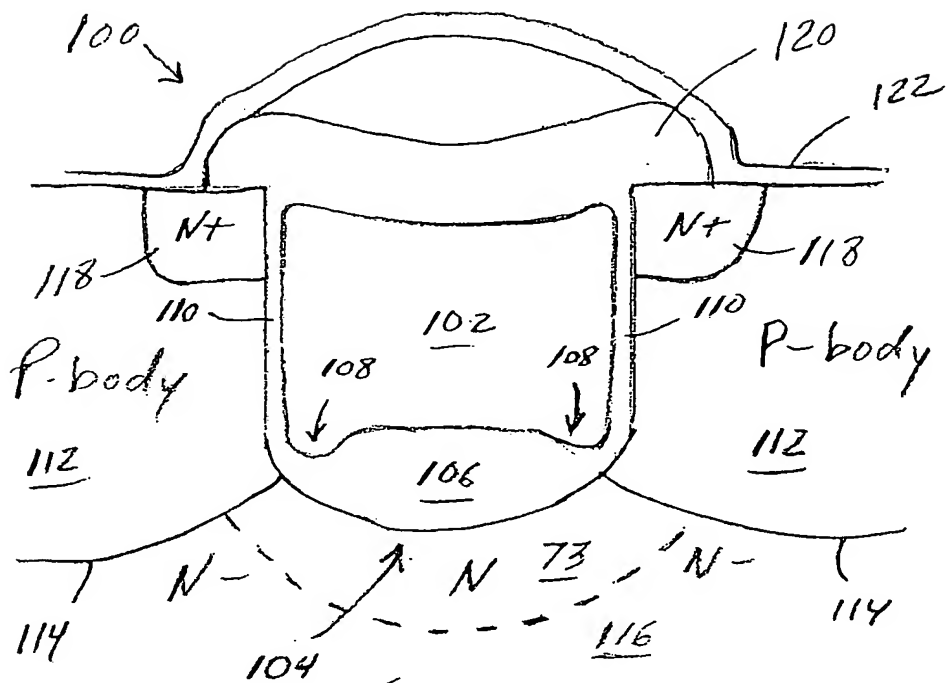


Fig. 10

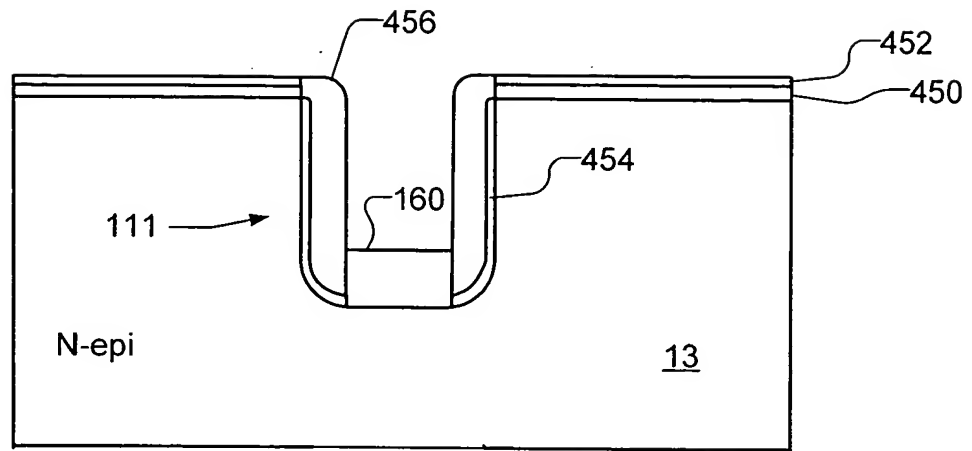


Fig. 11A

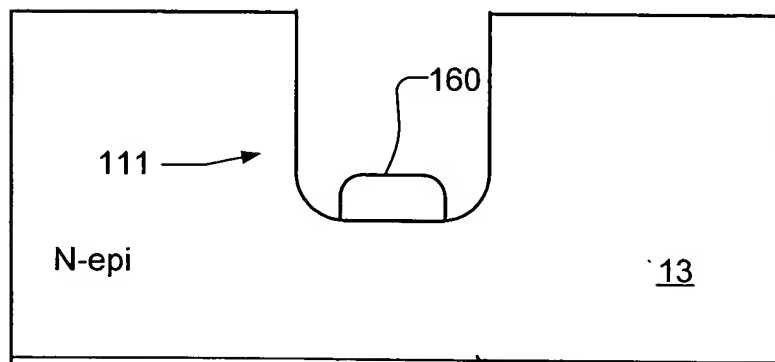
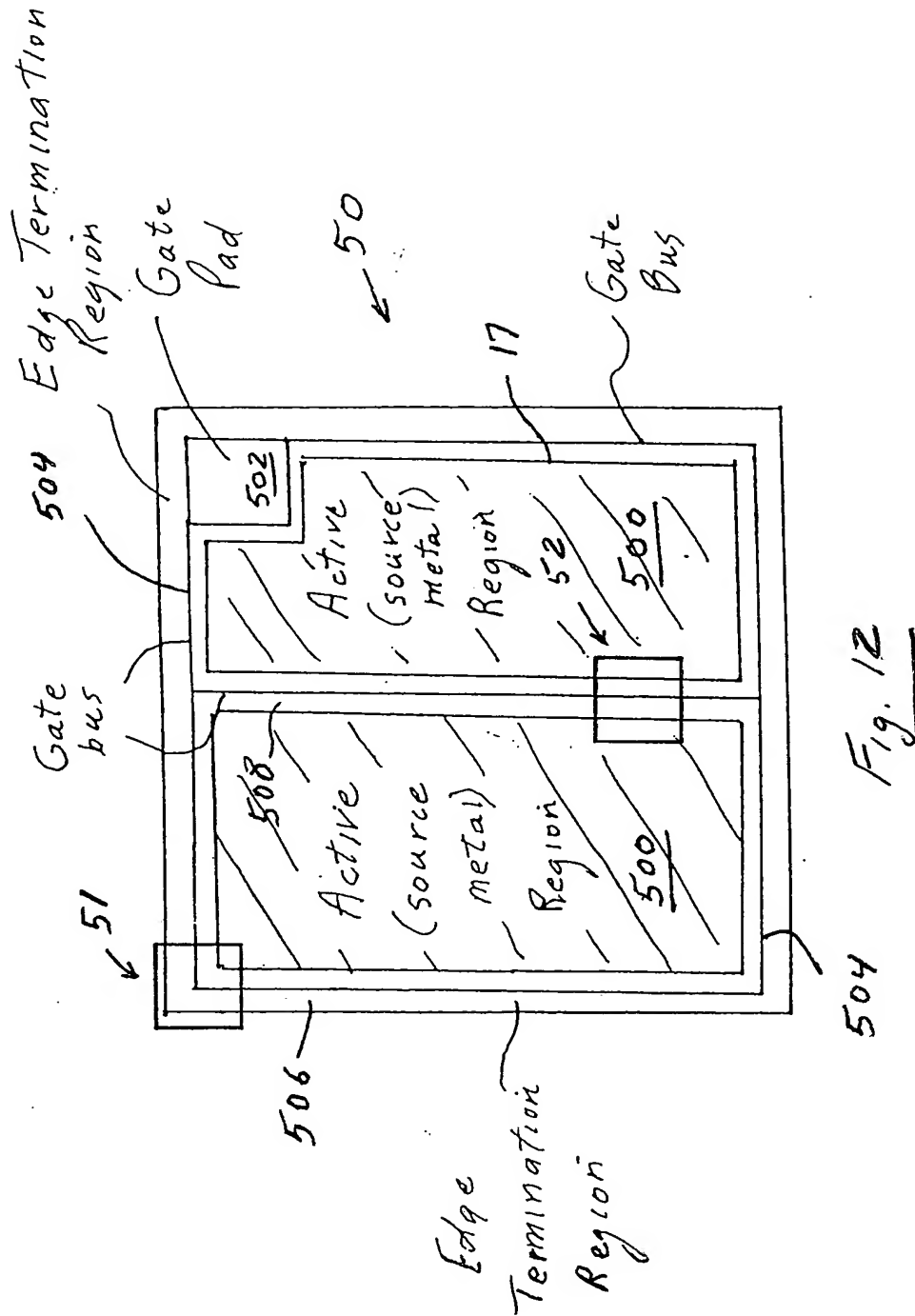


Fig. 11B



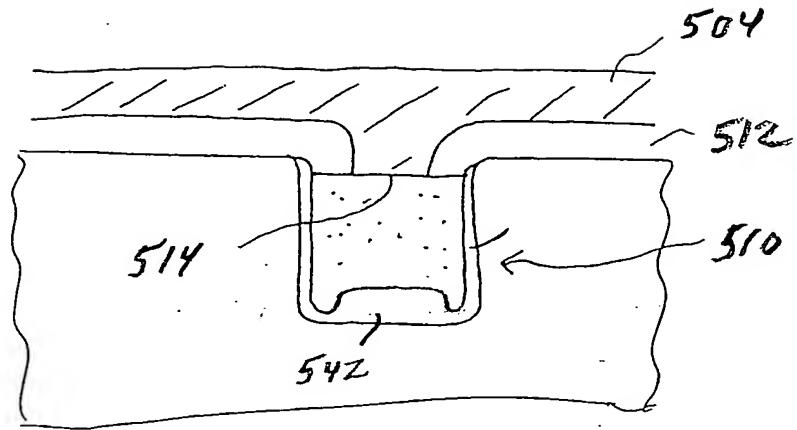
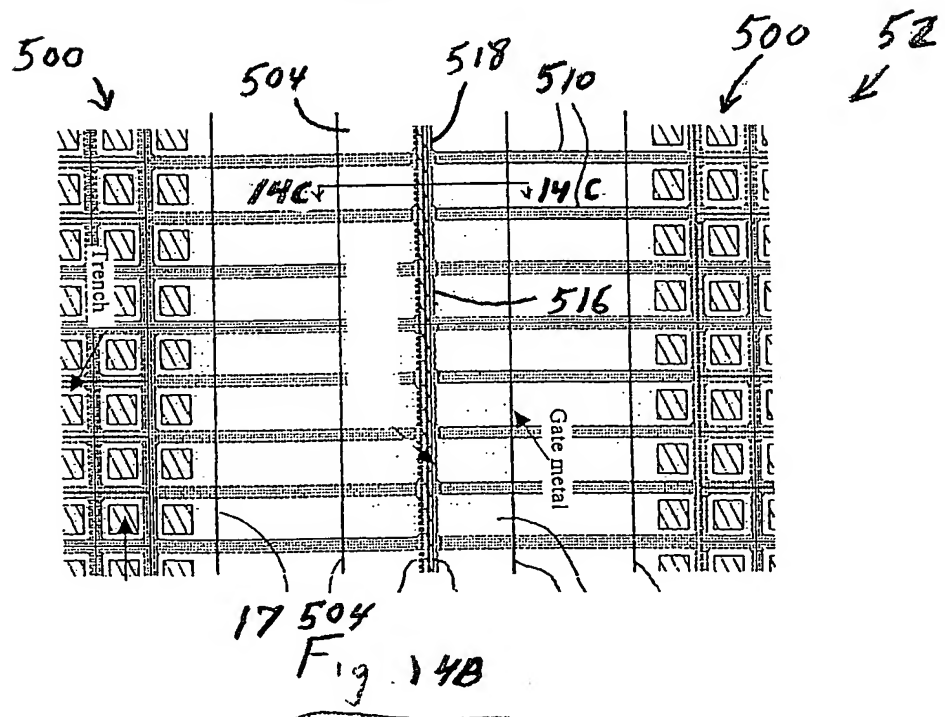
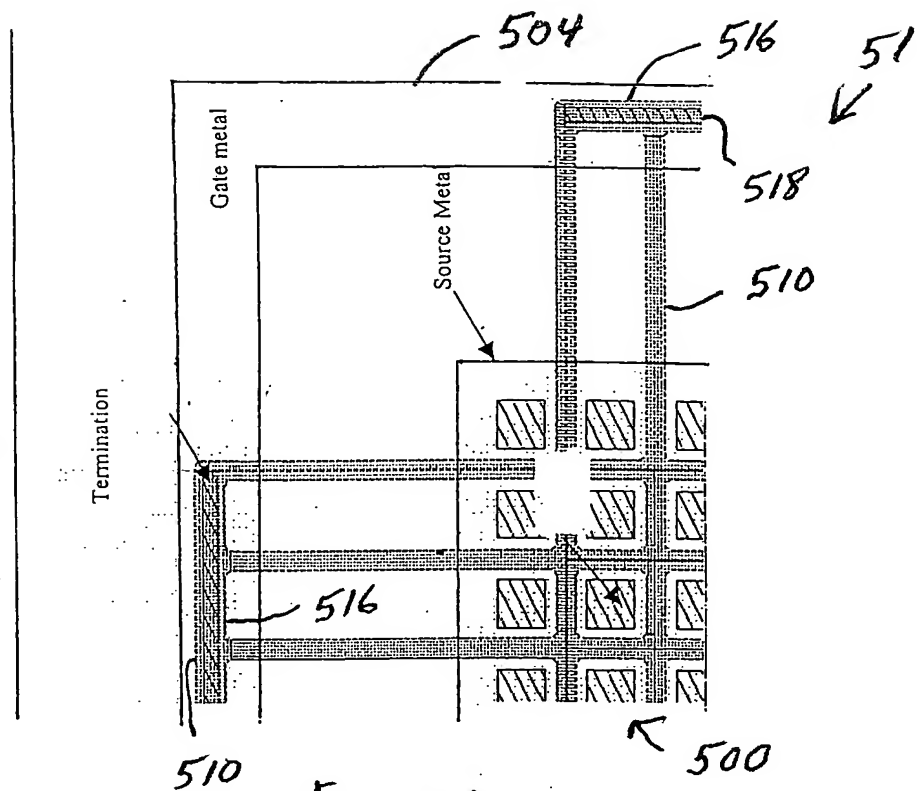


Fig 13C



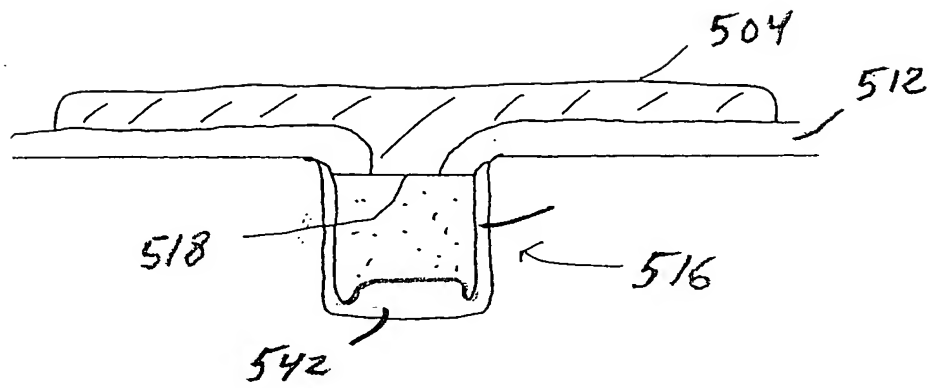


Fig 14C

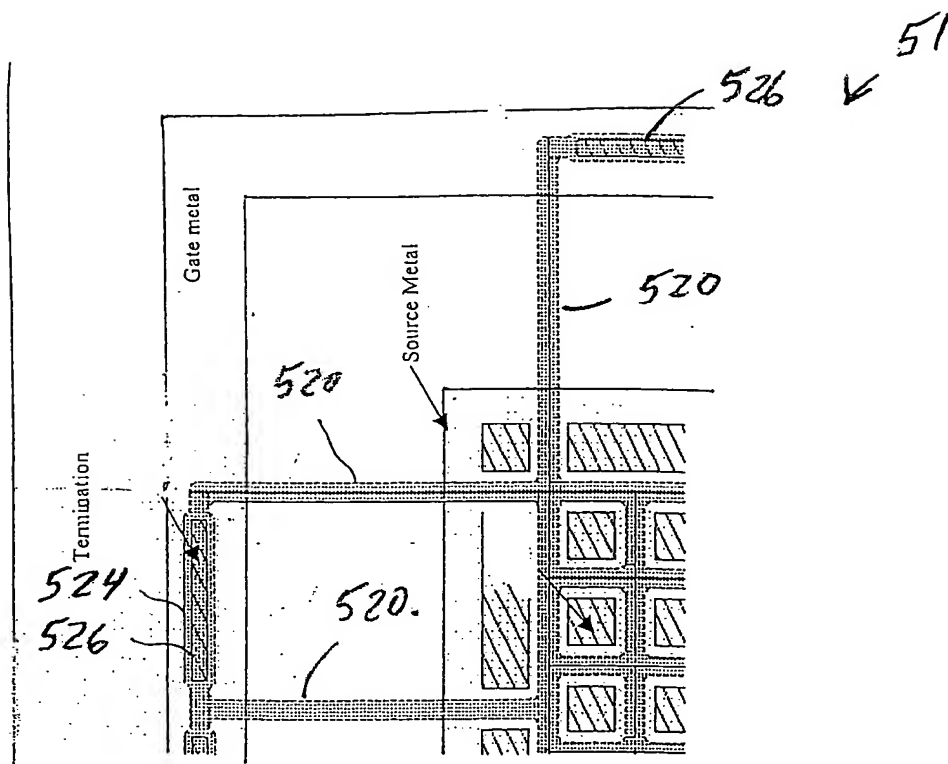


Fig. 15A

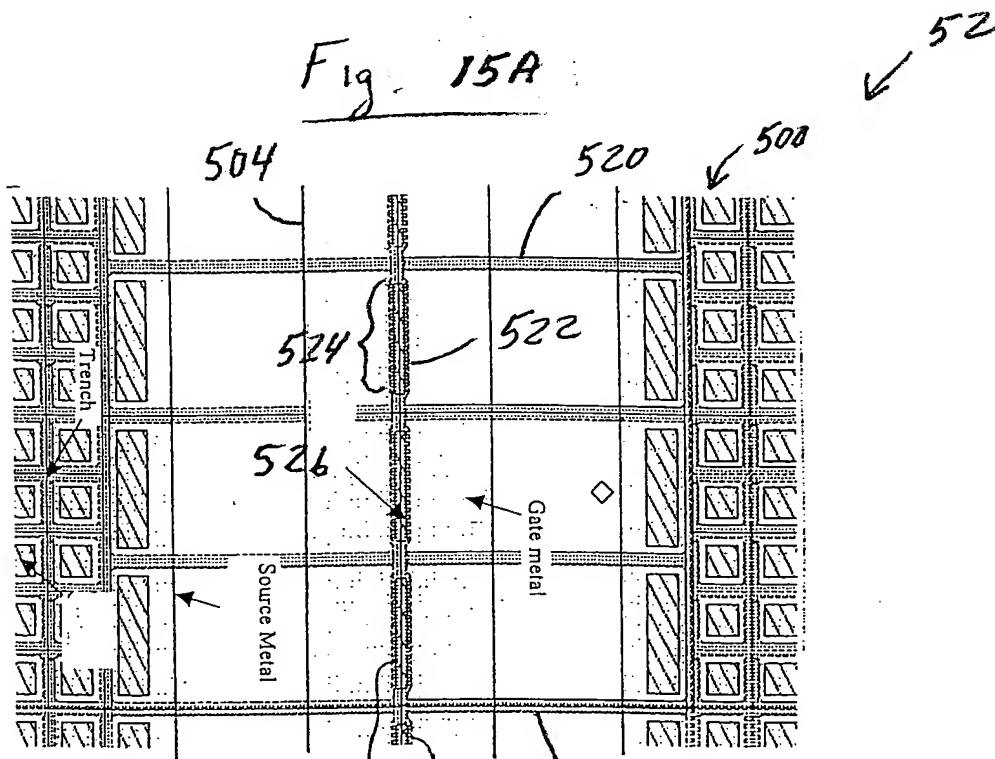


Fig. 15B

